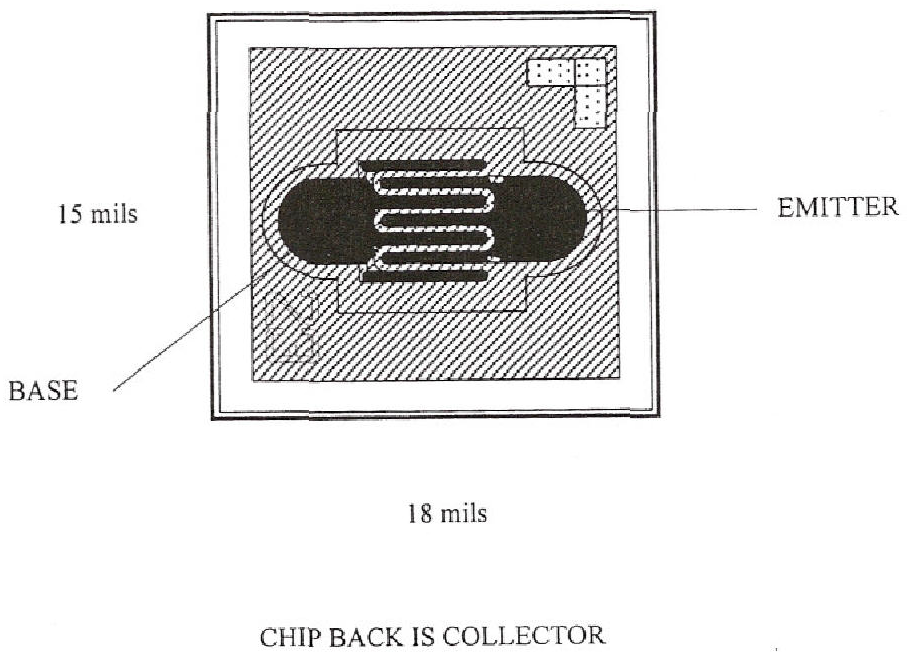
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.018”**



**E**

**B**

**.015”**

**CHIP BACK IS COLLECTOR**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” Min.**

**Backside Potential: Collector**

**Mask Ref: 004842**

**APPROVED BY: DK DIE SIZE .015” X .018” DATE: 10/18/21**

**MFG: NATIONAL SEMI THICKNESS .008” P/N: 2N3904**

**DG 10.1.2**

#### Rev B, 7/19/02